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suitably simple!

AM335x PRU-ICSS Debug

Introduction to the Programmable Real-
Time Unit (PRU) Training Series

~~Embedded Linux course Part 2:~~

~~AM335x Functional Overview~~

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Demonstrating Simple Open Real-Time Ethernet Protocol (SORTE) Master and Slave on PRU-ICSS using Pro
~~How to start development on the Sitara AM335x Starter Kit~~
How to Use the PRU to Control a Peripheral:
PRU_ADC_onChip on Sitara 335x using Beaglebone Black **MYD-**

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AM335x Development Board based on TI AM335x processor

Programmable Real-time Unit for
Gigabit Industrial Communication
Subsystem (PRU-ICSSG):

Accelerators *Rebuilding PRU*

Firmwares on Target Using Sitara

Processors Demonstrating DDR-less

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EtherCAT Slave on AMIC110

*Programmable Real-time Unit for
Gigabit Industrial Communication*

Subsystem (PRU-ICSSG): Overview

Unboxing MYD-C335X-GW

Development Kit Based on TI AM335x

ARM Cortex A8 processor How to

Build an SD Card with Processor SDK

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Linux Getting Started with the Beagle Bone Black Quick Start Guide -

ZCU104 Evaluation Kit What is

EtherCAT? ~~How to use GPIO pins on the Beaglebone Black Nuvoton~~

NuMaker NUC980 IIoT (1) – Install Development Environment

Porting U-Boot and Linux on New

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ARM Boards: A Step-by-Step Guide -
Quentin Schulz, Free Electrons
~~Lecture 15: Booting Process Special~~
~~Guest: Jason Kridner - BeagleBone~~
~~\u0026 PRU - TechTalk #038~~ How
Ethernet TCP/IP is Used by Industrial
Protocols Linux Development on the
Sitara AM335x and the MitySOM-335x

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Made Easy Start development with the
Sitara™ AM335x EVM

Demonstrating EtherCAT Master on
Sitara AM57x Gb Ethernet and PRU-
ICSSDemonstrating TI ESC SPI Mode
DDR-less AMIC110 with C2000
EtherCAT Slave Controlling and
Synchronizing Industrial Machines

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Using Real Time Ethernet

Programming BeagleBone Black

PRUs Chipsee Embedded Industrial

Computer - Opening the Box

Embedded Linux course Part 1 :

AM335x Functional Overview *Am335x*

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ListofFigures. 1 BlockDiagram..... 14 2

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PRU-ICSSIntegration

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As of Processor SDK Linux v6.1,
AM335x supports up to 6 additional
UARTs through PRU-ICSS GPIO pins.
The UART function is implemented in

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PRU firmware. The firmware is self-contained in the same PRU, which means the firmware does not use shared resources within an ICSS including IEP timer and Scratchpad.

*3.5. PRU-ICSS / PRU_ICSSG —
Processor SDK Linux Documentation*

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Simple PID Control Reference Design
With PRU®-ICSS Through Web
Interface Thermal Printing with the
PRU-ICSS on the BeagleBone Black
Reference Design Simple Open Real-
Time Ethernet (SORTE) Device With
PRU-ICSS Reference Design EnDat
2.2 System Reference Design.

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Evaluation Hardware . can be ordered
from ti.com. PRU Cape; Getting
Started Guide

PRU-ICSS - Texas Instruments Wiki
AM335x PRU-ICSS Reference Guide
The documentation on the subsystem
is here. TI does not support this

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subsystem and all questions/inquires/problems should be directed to the community. Example for the first PRU version (Ti AM18XX and other DSP)

<http://www.ti.com/tool/sprc940>

Ti AM33XX PRUSSv2 - eLinux.org

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----- The AM335x PRU Package includes: Documentation: AM335x PRU-ICSS overview slides AM18x to AM335x PRU software migration guide AM335x PRU Linux Application Driver documentation CCS AM335x PRU Debugger training slides AM335x_PRU_ICSS gel file for use

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with CCS AM335x PRU Debugger
PRU software (pru_sw): Utils: PASM
(PRU assembler) binary PASM ...

GitHub -

beagleboard/am335x_pru_package

As you have already discovered, the PRU GPI/Os are uni-directional (not bi-

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directional) and while some of the PRU GPIOs and GPOs are muxed on the same pin, the PRU does not have privileges to write to the AM335x Control Registers to change the pinmuxing. However, you could use the PRU Digital I/Os to achieve a high impedance output.

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AM335X: PRU access to pinmux settings - Processors forum ...

PRU-ICSS Ethernet/IP package is designed for the Sitara processor family (with PRU-ICSS IP) to enable customers add Ethernet/IP Adapter support to their system. The

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implementation consists of. Firmware (provided as a binary) Driver. PTP Driver; EtherNet/IP Driver (includes DLR) Application; There are plenty of resources to get started with the ...

*3.1. PRU ICSS EthernetIP User Guide
— PRU-ICSS Industrial ...*

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As seen from the screenshot the interrupt number for PRU_ICSS_EVTOUT_0 on AM335x is 20, so the interrupt number that must be configured for this in application should be 20 if the platform is AM335x. This is done in the following line (defined in main.c)

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*ICSS EMAC LLD developers guide -
Texas Instruments Wiki*

Parameters Arm MHz (Max.) 800

Serial I/O CAN, I2C, SPI, UART, USB

Co-processor(s) PRU-ICSS Graphics
acceleration 1 3D Ethernet MAC

2-Port 10/100 PRU EMAC, 2-Port 1Gb

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Switch Security enabler Cryptographic acceleration, Debug security, Initial secure programming, Secure boot, Software IP protection Operating temperature range (C)-40 to 105 Display type 1 LCD DRAM DDR2, DDR3, DDR3L, LPDDR Arm CPU ...

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*AM3359 data sheet, product
information and support | TI.com*

Parameters Arm MHz (Max.) 600, 800,
1000 Serial I/O CAN, I2C, SPI, UART,
USB Co-processor(s) PRU-ICSS
Graphics acceleration 1 3D Ethernet
MAC 2-Port 10/100 PRU EMAC,
2-Port 1Gb Switch Security enabler

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Cryptographic acceleration, Debug
security, Initial secure programming,
Secure boot, Software IP protection
Operating temperature range (C)-40 to
105, 0 to 90 Display type 1 LCD
DRAM DDR2, DDR3 ...

AM3358 data sheet, product

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information and support | TI.com

The description of the HIEISR register (AM335x PRU-ICSS Reference Guide chapter 6.4.9) is a bit unclear for me: The Host Interrupt Enable Indexed Set Register allows enabling a host interrupt output. The host interrupt. to enable is the index value written.

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*PRUSSV2 timer interrupt handling
example for AM335x*

Refer to the AM335x PRU ICSS
Reference Guide about these register
values. Each register is directly
addressable as a memory segment,
given by the Local Data Memory Map

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in the Reference Manual. This shows the IEP timer starts at address 0x0002_E000. The memory offset of the GLOBAL_CFG register is 0h (so no offset).

Beaglebone PRU Coding in C - GitHub Pages

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The Programmable Realtime Unit–Industrial Communications Sub-System (PRU-ICSS) is a versatile component of the AM335x SoC that enables real-time, deterministic Input and Output, even when running a non-realtime operating system. This reference design provides a concrete

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use case and implementation

*Thermal Printing With the PRU-ICSS
on the BeagleBone Black ...*

The Programmable Real-Time Unit
and Industrial Communications
Subsystem (PRU-ICSS / PRU-ICSSG)
is a small processor that is tightly

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integrated with an IO subsystem, offering low-latency control of IO pins on TI's SoC devices including the AM335x, AM437x, AM57x, and AM65x Sitara Processors. The PRU-ICSS / PRU-ICSSG is customer-programmable and can be used to implement simple and flexible control

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functions, peripherals, and state machines that directly access IO pins of the device, as well ...

Programmable Real-Time Unit and Industrial ... - TI.com

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Rev A - Orris

Table 1. Line-by-line for shared.pru0.c;
Line Explanation; 7. PRU_SRAM is defined here. It will be used later to declare variables in the Shared RAM location of memory. Section 5.5.2 on page 75 of the PRU Optimizing C/C++ Compiler, v2.2, User's Guide gives

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details of the command. The PRU_SHARED MEM refers to the memory section defined in am335x_pru.cmd on line 26.

Building Blocks - Applications

Host to PRU (ARM CortexA8 to PRU)

Interrupts Each PRU has access to

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host interrupt channels Host0 and Host1 through register R31 bit 30 and bit 31 respectively.

Ti AM33XX PRUSSv2 - SIUE

Information on the PRU is inconveniently split between the TRM and the AM335x PRU-ICSS Reference

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Guide. For specifics on the AM3358 chip used in the BeagleBone, see the 253 page datasheet. Texas Instruments' has the PRU wiki with more information.

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